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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,538	11/07/2001	Luca Battu'	851763.420	2722

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 04/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,538	BATTU' ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *1/20/06*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-16 are pending.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on 11/07/2000. It is noted, however, that the Examiner is unable to locate a certified copy of the 00830735.7 application as required by 35 U.S.C. 119(b). At this time, the Examiner is requesting a replacement certified copy of the priority document.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 3/22/02 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Arguments

Applicant's arguments filed 1/20/06 have been fully considered but they are not persuasive.

1. The Applicant has presented the following arguments:

a. Allen does not disclose, teach, or suggest emulation at the hardware level corresponding to an abstraction level of the digital circuit, such as the gate level or at the RTL level.

b. Allen does not provide any sort of "additional element" at all, at a hardware abstraction level, to perform power estimation.

c. Allen does not disclose, teach, or suggest detection of the number of transitions performed by the functional element during the time interval.

d. Allen's use of duty cycle is not tied to a specific given time interval.

2. Regarding the above arguments, the Examiner asserts:

a. In response to the applicant's argument that Allen does not disclose emulation at the hardware level corresponding to an abstraction level of the digital circuit, the examiner asserts that Allen discloses emulation at the hardware level corresponding to an abstraction level of the digital circuit, such as the gate level or at the RTL level (column 2 lines 35-59; column 3 lines 55-61). The specification cites that the invention may be configured either in the form of a processing unit of a dedicated type (such as a processor or a microprocessor) directly associated to the emulator, or in the from of a general-purpose digital computer which, appropriately programmed, implements the steps of the

invention (specification page 4). Accordingly, the prior art discloses a tool that utilizes a computer for estimating the power consumption of a circuit design that is described at the RTL or gate level (abstract; column 2 lines 26-33). The prior art discloses associating at least a portion of the RTL elements in the electrical design with at lest one of the plurality of power modules and generating a sum of power consumed by the RTL elements.

b. In response to the applicant's claimed argument that Allen does not disclose any sort of "additional element" at all, at a hardware abstraction level, to perform power estimation, the examiner asserts that Allen discloses the use of power estimation modules at a hardware abstraction level to measure the power consumed by the electrical design (column 8 lines 36-51, 56-60; (column 10 lines 42-45; column 13 lines 19-30). In view of the claim language, the 'additional element' is interpreted to be a power estimation module that is able to detect transitions in a signal value and use this to estimate the power consumed by a circuit.

c. In response to the applicant's argument that Allen does not disclose detection of the number of transitions performed by the functional element during the time interval, the examiner asserts that Allen discloses measuring the toggle rate, which is the number of transitions of a signal divided by the time over which the transitions were accumulated (column 10 lines 34-36).

d. In response to the applicant's argument that Allen's use of duty cycle is not tied to a specific given time interval, the examiner asserts that Allen discloses measuring

the duty cycle, which is defined as the percentage of time a signal is in an active state (column 10 lines 28-40). Therefore, the signal must be measured over a specific given time interval in order to calculate the percentage of time during which it is active.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. **Claims 1-16** are rejected under 35 U.S.C. 102(e) as being anticipated by Allen et al (US Patent No. 6,151,568), herein referred to as Allen.

As per **claims 1, 10, and 13**, Allen is directed to a process and system for estimating power consumption (column 1 lines 7-8) over a given time interval (column 10 line 51) of digital circuits (column 2 lines 26-27) described at the level of simulated functional elements (column 1 lines 8-11) provided with input/output terminals (column 3 lines 64-67, column 4 line 1), the process comprising:

a. estimating the power consumption based on a number of transitions performed by the simulated functional element during said time interval (column 10 lines 34-36; column 8 lines 36-51, 56-60). Allen discloses measuring the toggle rate, which is the number of transitions of a signal divided by the time over which the transitions were accumulated. The toggle data is part of the activity data, which is utilized by the power estimation module to calculate the consumed power (column 8 lines 56-60).

b. Emulating, at the hardware level corresponding to an abstraction level of the digital circuit (column 2 lines 35-39; column 3 lines 55-61; column 4 lines 7-11, lines 26-34), additional elements associated to said functional elements; said additional emulated elements being able to detect, during emulation of the circuit, at least one signal indicative of the behavior, and hence of power consumption (column 13 lines 19-30), of the corresponding functional element associated during said time interval (column 2 lines 33–39).

c. Acquiring the value of said at least one signal, said value being indicative of the power consumption of said associated functional element in said given time interval (column 2 lines 55-61).

Regarding claim 13, Allen discloses a logic module, analysis module, and multiple power modules (column 2 lines 34-39). The logic modules are used to represent the electrical design (column 2 lines 45-50). The analysis module associates at least a portion of the RTL elements in the electrical design with one of the power modules. The analysis module is responsible for the

measuring of the signals (column 2 lines 55-61) so it may then calculate the consumed power (column 2 lines 62-67).

As per **claim 2**, Allen is directed to the process according to claim 1, wherein said additional elements are emulated by associating them to an output of the functional element (column 9 lines 47-57).

As per **claims 3 and 11**, Allen is directed to the process and system according to claim 1 and 10, respectively, wherein said additional emulated elements are able to detect, during said given time interval:

a. a fraction of time in which the state of the corresponding associated functional element is stable (column 10 lines 38-40). The Illustrated Dictionary of Electronics defines stability as "the condition in which an equipment or device is able to maintain a particular mode of operation without deviation" (Gibilisco 652). The examiner interprets "a particular mode of operation without deviation" to mean a state where the device is set high for a set period of time. Allen's discloses a process where the simulator measures the duty cycle, which is defined by the Illustrated Dictionary of Electronics as "the proportion of percentage of time during which a device, circuit, or system is operating or handling power" (Gibilisco 220). The examiner interprets "operating" to mean a state when the device is set high for a set period of time. Thus the duty cycle measured in Allen's invention and the stability measured in the claimed invention are equivalent. The

duty cycle is part of the activity data, which is utilized by the power estimation module to calculate the consumed power (column 8 lines 56-60).

b. The value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval (column 10 lines 28-40; column 14 lines 7-10). Therefore, the signal must be measured over a specific given time interval in order to calculate the percentage of time during which it is active.

As per **claim 4**, Allen is directed to the process according to claim 1, further comprising controlling acquisition of the value of said at least one signal using hardware events monitored by logic analyzers active on the additional elements (column 10 lines 25-36; column 8 lines 36-51). The power module contains a transition section that monitors the transitions of the signals (i.e. changes in the signal value).

As per **claim 5**, Allen is directed to the process according to claim 1, further comprising accessing the information stored in said additional emulated elements and storing said information (column 14 lines 28-30) in view of subsequent processing (column 4 lines 33-38).

As per **claim 6**, Allen is directed to a processing system to implement the process according to claim 1 (column 5 lines 18-19).

As per **claim 7**, Allen is directed to a computer program product directly loadable into the internal memory of a digital computer, comprising software code portions for performing the steps of claim 1 when said product is run on a computer (column 2 lines 27-32).

As per **claims 8, 12, and 16**, Allen is directed to the process, system and apparatus of claims 1, 10, and 13 respectively, wherein emulating at the hardware level includes emulating at a register transfer level (column 2 lines 32-33).

As per **claims 9, 12, and 16**, Allen is directed to the process, system and apparatus of claims 1, 10, and 13 respectively, wherein emulation at the hardware level includes emulating at a gate level (column 2 lines 55-61).

As per **claim 15**, Allen is directed to the apparatus of claim 13, wherein the third module includes machine-readable instructions stored on a machine-readable medium and executable by a processor (column 5 lines 18-25).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KAMINI SHAH
SUPERVISORY PATENT EXAMINER